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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,736	03/31/2004	Richard Nigel Chamberlain	GB920030066US1	7236

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IBM Corporation
IP Law Department
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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,736	CHAMBERLAIN ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-25* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/814,736 has a total of 25 claims pending in the application; there are 4 independent claims and 21 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required bye **M.P.E.P. 201.14(c)**, acknowledgement is made of applicant's claim for priority based on applications filed on 11/5/03 (United Kingdom – 0325788.8).

III. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

IV. OBJECTIONS TO THE SPECIFICATION

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The following title is suggested: -- **Memory Allocation Using Mask-Bit Pattern to Encode Metadata Within Memory Address** --.

V. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. **Claims 20-23 and 25** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

8. As per **claims 20-21**, Applicant has claimed a "program element" in the preamble to these claims; this implies that Applicant is claiming a system of software, per se, lacking the hardware necessary to realize any of the underlying functionality; therefore, these claims are directed to nonstatutory subject matter.

9. As per **Claims 22-23**, these claims recite the limitation of "a carrier medium;" therefore, claims 22-23 are directed to non-statutory subject matter as these claims recite nothing more than a transmission media to transfer signals which are defined as physical characteristics of a form of energy, such as frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory phenomena. Moreover, it does not appear that a claim reciting a signal encoded with function descriptive material falls within any of the categories of patentable subject matter set forth 35 U.S.C. 101.

10. As per **claims 20-23 and 25**, these claims recite the limitation of "a program product directly loadable into the internal memory of a digital computer" or a "program element" which, Applicant's specification defines as "an electronic signal," or a "radio frequency carrier wave carrying suitable encoded signals representing the computer program and data" (page 12, lines 12-23). Therefore, claims 20-23 and 25 are directed to non-statutory subject matter as these claims recite nothing more than a transmission media to transfer signals which are defined as physical characteristics of a form of energy, such as frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are nonstatutory phenomena. Moreover, it does not appear that a claim reciting a signal encoded with function descriptive material falls within any of the categories of patentable subject matter set forth 35 U.S.C. 101.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. **Claims 1-3, 8-12, 15-16, 19-25** are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi (US 5,706,469).

13. As per **claims 1, 15, 20-23 and 25**, Kobayashi discloses "A method/mechanism of allocating memory in a data processing system having a memory, the method

comprising the steps of:" as **["a data processing system capable of controlling bus access to a memory area of an arbitrary size with the use of a small number of registers" (Column 2, lines 19-21)]** "receiving a memory allocation request from a running process, the request including data relating to the size of the block of memory required and an indication of a mask bit pattern;" **[Kobayashi discloses this concept as "the microprocessor 1, whenever it becomes necessary to make access to memory 3, sends information required for the access including an access request generated in an internal data arithmetic section or the like together with the address, data length, direction of transfer (read/write) and, appropriate data in the case of a write cycle" (Column 8, lines 60-66) and explains that "a signal indicating that the most significant bits in the to-be-accessed address which are not masked by the mask bits coincide with the most significant bits of the head address set in the memory area address register is output to the memory controller decoding the address as a signal for specifying the memory area to be accessed" (Column 2, lines 53-59); wherein "as a result, the head address of the memory area of a size designated by the mask bits and containing the address to be accessed is extracted from the particular address" (Column 9, lines 18-21) as having both, a size of a memory block to be accessed and mask bit pattern within a memory allocation request]** "selecting a block of memory of appropriate size and having an address including a bit pattern corresponding correctly to the mask bit pattern; and allocating the selected block of memory to the process" **[With respect to this limitation, Kobayashi discloses having EX-NOR gates to check whether**

masked bits coincide with a memory address register (Column 9, lines 22-34); providing an example in which a "to-be-accesses address" corresponds to area 1 on the memory space and explains that "the memory controller 2" decodes the most significant 4 bits of the to-be-accessed address wherein "a MEM(1)# signal means that the most significant four bits of the address coincide with the most significant four bits of the memory are address register (1)" (Column 9, lines 45-57) as providing the necessary steps for selecting a memory are to be accessed].

14. As per **claims 2, 16 and 24**, Kobayashi discloses "A method/mechanism according to claims 1 and 15," **[See rejection to claim 1 above]** "further comprising the step of the process sending the memory allocation request to a memory allocation mechanism" **[With respect to this limitation, Kobayashi discloses that "An access via a bus is initiated by the microprocessor asserting a strobe signal indicating the start of bus access. A memory controller receives an address and the strobe signal from the microprocessor, decodes the address signal, accesses a memory associated with the decoded address, and returns an access completion signal to the microprocessor at a predetermined timing when completing the access" (Column 1, lines 16-21) as having a memory controller performing a memory allocation mechanism]**.

15. As per **claim 3**, Kobayashi discloses "A method according to claim 1," **[See rejection to claim 1 above]** "wherein the step of allocating the selected block comprises sending an allocation reply to the process, the allocation reply indicating the address of the selected memory block" **[Kobayashi discloses this limitation as "a**

signal indicating that the most significant bits in the to-be-accessed address which are not masked by the mask bits coincide with the most significant bits of the head address set in the memory are address register is output o the memory controller decoding the address as a signal for specifying the memory area to be accessed" (Column 2, lines 54-59)].

16. As per **claim 8**, Kobayashi discloses "A method according to claim 1," **[See rejection to claim 1 above]** and also teaches a prior art example in which "the selecting step comprises splitting a memory block larger than the requested size into two or more blocks" as **["an address range valid on the memory can be set for each 256 MB obtained by dividing a 32-bit address space (4 GB) equally into 16 areas" (Figure 3 and Column 1, lines 57-60)]**; further disclosing "blocks having an appropriate size for the memory allocation and having a memory address including a bit pattern which corresponds correctly to the mask bit pattern" **[See rejection to claim 1]**.

17. As per **claim 9**, Kobayashi discloses "A method according to claim 1," **[See rejection to claim 1 above]** "further comprising the step of the process selecting a mask bit pattern" **[With respect to this limitation, Kobayashi discloses "In bits 0 to 19 of the memory area mask register are assigned mask bits (third bit string) for masking a predetermined number of least significant ones of the most significant 20 bits of the address to be accessed in accordance with the size of the memory area to be designated and thus specifying the size of memory areas 0 to 3" (Column 8, lines 14-19) as selecting/providing different mask bit patterns for accessing different areas of memory]**.

18. As per **claims 10, 11 and 19**, Kobayashi discloses "A method according to claims 1 and 15," **[See rejection to claims 1 and 15 above]** "wherein the indication of the mask bit pattern comprises a mask, specifying certain bits of an address, and a set of values indicating the required value for each of the specified bits" **[Kobayashi discloses this concept as "a bit pattern shown in Fig. 17 is assigned to the register set of four entries" (Column 8, lines 26-27) and explains that "in bits 0 to 19 of the memory area mask register are assigned mask bits (third bit string) for masking a predetermined number of least significant ones of the most significant 20 bits of the address to be accessed in accordance with the size of the memory area to be designated and this specifying the memory areas 0 to 3" (Column 8, lines 14-19)]** "wherein the step of selecting a memory block includes checking whether each of the certain bits of the memory address of a free block corresponds correctly to the required value indicated in the memory allocation request" **[Kobayashi discloses this concept as "a signal indicating that the most significant bits in the to-be-accessed address which are not masked by the mask bits coincide with the most significant bits of the head address set in the memory area address register is output to the memory controller decoding the address as a signal for specifying the memory area to be accessed" (Column 2, lines 53-59)]**.

19. As per **claim 12**, Kobayashi discloses "A method according to claim 1," **[See rejection to claim 1 above]** "further comprising the step of the process storing data in the allocated memory" **[Kobayashi discloses this concept as "the microprocessor 1, whenever it becomes necessary to make access to the memory 3, sends**

information required for the access including an access request generated in an internal data arithmetic section or the like together with the address, data length, direction of transfer (read/write) and, appropriate data in the case of a write cycle" (Column 8, lines 60-66) as providing a write cycle which would store data in an allocated memory area].

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (US 5,706,469) in view of Kirk, III. (US 6,421,690).

22. As per **claim 4**, Kobayashi discloses "A method according to claim 1," **[See rejection to claim 1 above]** and also discloses having one or more bits of metadata assigned to each memory address as **["the single bit (BW), the bus error bit (BE) and the burst transfer mode bit (BM), etc. are assigned to the memory area address register in the foregoing embodiments, an effect similar to that of the present embodiment is obtained when these bits are assigned to the memory are mask register" (Column 15, lines 43-53) as explaining that flag bits may also be provided within a mask register used to mask memory addresses]** but does not disclose expressly "embedding metadata into the address of the allocated block of memory, and storing the encoded address".

Kirk discloses "embedding metadata into the address of the allocated block of memory, and storing the encoded address" as **["a Generic Memory Management System which defines relational schemes for memory pointers in object-based computer systems" and "includes a set of attributes associated with system references (pointers), thus creating a set of "smart pointers." The attributes preferably are effected through a set of flags associated with the pointers" (Column 2, lines 44-54)]**.

Kobayashi (US 5,706,469) and Kirk, III. (US 6,421,690) are analogous art because they are from the same field of endeavor of computer memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the memory allocation system which uses a mask bit pattern to select a to-be-accessed memory area as disclosed by Kobayashi and further embed one or more flags within an address or pointer as taught by Kirk.

The motivation for doing so would have been because Kirk teaches that embedding flags within a memory pointer allows **["a designer to efficiently determine how memory management will occur" (Column 3, lines 3-4) as smart pointer flags "provide enhanced memory managements functionality" wherein, for example, these flags "may be utilized to automatically determine when memory links may be broken, freeing up computer memory" (Column 1, lines 17-21)]**.

Therefore, it would have been obvious to combine Kirk, III. (US 6,421,690) with Kobayashi (US 5,706,469) for the benefit of creating a memory management system to obtain the invention as specified in claim 4.

23. **Claims 5 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (US 5,706,469) in view of Kirk, III. (US 6,421,690) as applied to claim 4 above, and further in view of Garthwaite et al. (US 7,016,923).

24. As per **claim 5**, the combination of Kobayashi and Kirk discloses "A method according to claim 4," **[See rejection to claim 4 above]** but fails to expressly disclose that the process of embedding metadata comprises "replacing certain bits of the address of the allocated block of memory with flag bits."

Garthwaite discloses embedding metadata by "replacing certain bits of the address of the allocated block of memory with flag bits" as **["the least significant bits are known to be zero an can be replaced by appropriate flags that indicate how the addresses should be treated" (Column 17, lines 40-44)]**.

Kobayashi (US 5,706,469), Kirk, III. (US 6,421,690) and Garthwaite (US 7,016,923) are analogous art because they are from the same field of endeavor of computer memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the memory allocation system which uses a mask bit pattern to select a to-be-accessed memory area as disclosed by Kobayashi, embed one or more flags within an address or pointer as taught by Kirk and further embed metadata into an address by "replacing certain bits of the address of the allocated block of memory with flag bits."

The motivation for doing so would have been because Garthwaite teaches that embed metadata into an address by "replacing certain bits of the address of the

allocated block of memory with flag bits" provides **[less consumption of memory space as this approach can be seen as "space-efficiently encoding" and also facilitates management/identification of data as it enables the distinction between "task items and list items as well as among different kinds of task items" (Column 17, lines 44-49)]**.

Therefore, it would have been obvious to combine Garthwaite et al. (US 7,016,923) with Kobayashi (US 5,706,469) and Kirk, III. (US 6,421,690) for the benefit of creating a memory management system to obtain the invention as specified in claim 5.

25. As per **claim 13**, Kobayashi discloses "A method of performing a memory update in a data processing system having a memory," as **["a data processing system capable of controlling bus access to a memory area of an arbitrary size with the use of a small number of registers" (Column 2, lines 19-21) and explains that "the microprocessor 1, whenever it becomes necessary to make access to memory 3, sends information required for the access including an access request generated in an internal data arithmetic section or the like together with the address, data length, direction of transfer (read/write) and, appropriate data in the case of a write cycle" (Column 8, lines 60-66) as writing/updating data]** "the method comprising the steps of: reading an encoded memory address from memory;" **[With respect to this limitation, Kobayashi discloses "a signal indicating that the most significant bits in the to-be-accessed address which are not masked by the mask bits coincide with the most significant bits of the head address set in the memory**

area address register is output to the memory controller decoding the address as a signal for specifying the memory area to be accessed" (Column 2, lines 53-59); wherein "as a result, the head address of the memory area of a size designated by the mask bits and containing the address to be accessed is extracted from the particular address" (Column 9, lines 18-21)] but fails to disclose "determining whether one or more flag bits embedded in the encoded memory address are set;" and "resetting one or more of the flag bits in the encoded memory address; and storing the updated encoded memory address in the memory."

Kirk discloses having flags embedded in encoded memory address and setting/resetting these flags as **["a Generic Memory Management System (GeMS) which defines relational schemes for memory pointers in object-based computer systems" and "includes a set of attributes associated with system references (pointers), thus creating a set of "smart pointers." The attributes preferably are effected through a set of flags associated with the pointers" (Column 2, lines 44-54) wherein "the behavior of the basic GeMS smart pointer can be controlled by setting or clearing certain flags contained within it. Having different flags set or cleared changes the characteristics of the relationship represented by the smart pointer" (Column 5, lines 46-50)]** but fails to discloses that the embedded flags within each memory address comprise one or more bits.

Garthwaite discloses embedding metadata by "replacing certain bits of the address of the allocated block of memory with flag bits" as **["the least significant bits**

are known to be zero an can be replaced by appropriate flags that indicate how the addresses should be treated" (Column 17, lines 40-44)].

Kobayashi (US 5,706,469), Kirk, III. (US 6,421,690) and Garthwaite (US 7,016,923) are analogous art because they are from the same field of endeavor of computer memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the memory allocation system which uses a mask bit pattern to select a to-be-accessed memory area as disclosed by Kobayashi, embed one or more flags within an address or pointer and set/clear these flags as taught by Kirk and further have these flags comprise one or more bits as taught by Garthwaite.

The motivation for doing so would have been because Kirk teaches that embedding flags within a memory pointer and setting/resetting these flags allows **["a designer to efficiently determine how memory management will occur" (Column 3, lines 3-4) as smart pointer flags "provide enhanced memory managements functionality" wherein, for example, these flags "may be utilized to automatically determine when memory links may be broken, freeing up computer memory" (Column 1, lines 17-21)]** and Garthwaite teaches that embedding metadata into an address by "replacing certain bits of the address of the allocated block of memory with flag bits" provides **[less consumption of memory space as this approach can be seen as "space-efficiently encoding" and also facilitates management/identification of data as it enables the distinction between "task**

items and list items as well as among different kinds of task items" (Column 17, lines 44-49)].

Therefore, it would have been obvious to combine Garthwaite et al. (US 7,016,923) with Kobayashi (US 5,706,469) and Kirk, III. (US 6,421,690) for the benefit of creating a memory management system to obtain the invention as specified in claim 13.

26. **Claims 6-7 and 17-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (US 5,706,469) in view of Frank et al. (US 5,860,144).

27. As per **claims 6-7 and 17-18**, Kobayashi discloses "A method according to claims 1 and 15," **[See rejection to claims 1 and 15 above]** wherein allocating a memory block comprises selecting a memory block having an address which corresponds correctly to the mask bit pattern **[See rejection to claims 1 and 15 above]** but does not disclose expressly "wherein a memory allocation mechanism has one or more list(s) of free memory blocks," and the selecting step comprises searching through a list of free blocks" and one or more lists of "allocated memory blocks and the allocation step comprises taking the selected block off a list of free memory blocks and adding the selected block to a list of allocated blocks."

Frank discloses a memory allocation mechanism has one or more list(s) of free memory blocks," and the selecting step comprises searching through a list of free blocks" and one or more lists of "allocated memory blocks and the allocation step comprises taking the selected block off a list of free memory blocks and adding the selected block to a list of allocated blocks" as **[a memory system which is capable of**

providing n-bit addressability (Column 3, lines 60-61) comprising "a free VACB list 346 which is coupled to VACB table 350 (*analogous to an allocation table*) and maintains a listing of all VACB entries within table 350 that are currently free (e.g. vacant)" (Column 10, lines 26-33) and explains removing entries from a free list and adding them to an allocation or "VACB table 350" when these entries are mapped/allocated to a process (Column 15, lines 13-22)].

Kobayashi (US 5,706,469) and Frank et al. (US 5,860,144) are analogous art because they are from the same field of endeavor of computer memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the memory allocation system which uses a mask bit pattern to select a to-be-accessed memory area as disclosed by Kobayashi, and further provide a list of free memory areas as well as a list of allocated memory areas wherein entries are removed from a free list and added to an allocated list in response to a memory allocation as taught by Frank.

The motivation for doing so would have been because Frank teaches that providing a list of free memory areas as well as a list of allocated memory areas wherein entries are removed from a free list and added to an allocated list in response to a memory allocation as taught by Frank **["substantially reduces memory overhead" and provides faster memory accesses (Column 17, lines 21-23, 45-47 and Column 18, lines 1-2) even for systems using different addressing modes such as 16, 32, 64 or n - bit modes]**.

Therefore, it would have been obvious to combine Frank et al. (US 5,860,144) with Kobayashi (US 5,706,469) for the benefit of creating a memory management system to obtain the invention as specified in claims 6-7 and 17-18.

VII. RELEVANT ART CITED BY THE EXAMINER

28. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

29. The following reference teaches a memory address decoding method to determine if a memory address is located within one of a plurality of sections.

U.S. PATENT NUMBER

US 2004/0172497

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

30. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

31. Per the instant office action, claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reasons for allowance of claim 14 in the instant application is the combination with the inclusion in these claims of the limitation of "**decoding the memory address by replacing the one or more embedded flag bits with bits of the memory address, in dependence on the mask bit pattern, and reading data from that memory address**." The prior art of record including the disclosures under section **VII** above neither anticipates nor renders obvious the above-recited combination.

a(2) CLAIMS REJECTED IN THE APPLICATION

32. Per the instant office action, claims 1-13 and 15-25 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

34. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 27, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER